REMARKS

Upon entry of the present amendment, claim 8 will have been canceled, without prejudice and without disclaimer of the subject matter, and claims 1-7 will have been amended to correct informalities in the claim language and to more clearly define the invention, while not substantially affecting or narrowing the scope of these claims. Further, claim 1 will have been amended to substantially incorporate the subject matter of canceled claim 8. Applicant respectfully submits that all pending claims are now in condition for allowance.

Furthermore, upon entry of the present amendment, the drawings will have been amended to include labels for the flow directions after the decision boxes 2802, 2805 and 2807 in Fig. 28 to indicate the decision that prompts the alternative flow directions, as discussed above. A corrected formal version of Fig. 28, which incorporates the amendments, is being submitted as part of the present Reply. No new matter has been introduced in the application by the amended drawings.

In the above-referenced Official Action, the Examiner rejected claim 8 under 35 U.S.C. § 112, first paragraph, asserting that the specification does not reasonably provide enablement for setting the comparison address data (*i.e.*, address data of the defective part in the ROM) as a return-address data in the program counter when the interruption-processing is completed. Initially, Applicant notes that the present invention is not limited to replacing a defective part in the ROM, as apparently implied by the Examiner. Rather, the present invention enables other revisional programming, including, for example, supplementing the ROM with additional code.

With respect to the merits of the rejection, Applicant submits that the specification is sufficiently enabling with respect to the subject matter of amended claim 1. For example, the

disclosure from page 47, line 9 to page 48, line 12, of the specification describes the functionality of setting the return-address to coincide with the comparison address data, when execution of the interruption process is completed, and to disable coincidence between the two, as discussed below. Therefore, Applicant respectfully requests the Examiner to withdraw the rejection under 35 U.S.C. § 112, first paragraph.

Also in the above-referenced Official Action, the Examiner rejected claims 1-5 under 35 U.S.C. § 102(e) as being anticipated by SHIMADA et al. (U.S. Patent No. 6,237,120). The Examiner rejected claims 6 and 7 under 35 U.S.C. § 103(a) as being unpatentable over SHIMADA et al. Applicant respectfully traverses these rejections, at least for the reasons stated below.

As previously noted, the subject matter of canceled claim 8 has been substantially incorporated into independent claim 1. Claim 8 was generally directed to the address coincidence disabling functionality of the address-coincidence-interruption-prohibiting register (ACIPR) 58 shown, for example, in Fig. 2 of the specification. Essentially, the AC signal output from address comparator 52 is ignored when flag data (FD1, FD2) held in the ACIPR 58 is set to "1." This enables the process of the claimed invention to restart from the address at which the interruption occurred. Also, the flag data may be controlled by the revisional program. See, e.g., page 47, line 9 to page 48, line 12, of the specification. Consequently, because the process returns to the interruption address, new instructions can be simply inserted between two succeeding instructions without skipping the instruction assigned to the interruption address.

In comparison, SHIMADA et al. appear to teach that the process returns to an address next to the address at which the interruption occurred. Therefore, an instruction assigned to the

interruption address is never executed. See, e.g., col. 4, lines 42-52. To avoid skipping the instruction assigned to the interruption address, the instruction must be rewritten and added to the revisional program. This wastes memory, especially when the rewritten instruction requires more than one byte of memory. Further, Applicant notes that the Examiner did not identify any portion of SHIMADA et al. that teaches or suggests setting return-address data in the program counter to coincide with the comparison address data upon completion of the interruption-process, and/or disabling the coincidence between the comparison address data and the return-address set in the program counter, as recited in amended claim 1. Accordingly, Applicant respectfully submits that claim 1, as amended, is patentable over SHIMADA et al.

With regard to claims 2-7, Applicant asserts that they are allowable at least because they depend from independent claim 1, which Applicant submits has been shown to be allowable.

In view of the herein contained amendments and remarks, Applicant respectfully requests reconsideration and withdrawal of previously asserted rejections set forth in the Official Action of April 9, 2003, together with an indication of the allowability of all pending claims, in due course. Such action is respectfully requested and is believed to be appropriate and proper.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attached thereto.

Should the Examiner have any questions concerning this Reply or the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Hiroyuki TAKAHASHI

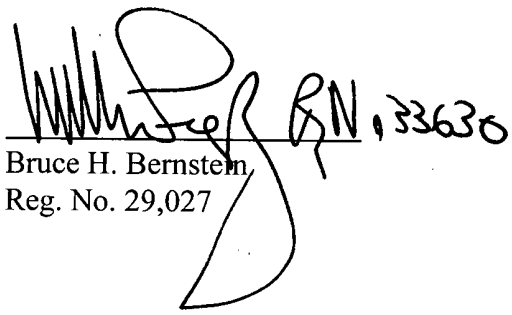

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FIG. 28